DESCRIPTION AMENDMENTS

Rewrite the paragraph beginning on page 6, line 11, to read as follows:

The above is illustrated in Fig. 3 where a series of frames of variable bit rates is shown. At time δ before the DTS for frame 1, frame 1 is loaded into the buffer. The buffer may be thought of as having a plurality of equal capacity slots between consecutive DTS times. Since frame 1 has fewer bits than the capacity of one slot, there is a gap before frame 2 is loaded into the buffer, again at time δ before the DTS for frame 2. Likewise frame 3 is loaded at time δ before DTS_3. Frame 3 has more bits than fit into one slot, so frame 4 is loaded into the buffer as soon as possible thereafter. Then frame 5 is loaded into the buffer as soon as possible. The end of frame 5 almost exceeds the DTS time for frame 5 and the buffer is in danger of overflowing. However the next few frames 6, 7 and 8 each have fewer bits than one slot so the capacity of the buffer is alleviated.